

# 16-Channel/Dual 8-Channel JFET Analog Multiplexers (Overvoltage Protected)

MUX-16/MUX-28

#### **FEATURES**

- JFET Switches Rather Than CMOS
- Highly Resistant To Static Discharge Damage
- No SCR Latch-up Problems
- Low "ON" Resistance 290ΩTypical
- Low Leakage Current
- Digital Inputs Compatible With TTL and CMOS
- Break-Before-Make Action
- 125° C Temperature-Tested Dice Available
- Overvoltage Protected
- Supply Loss Protection
- MUX-16 Pin Compatible With DG506, HI-506A, AD7506
- MUX-28 Pin Compatible With DG507, HI-507A, AD7507
- Available in Die Form

# ORDERING INFORMATION †

		PACKAGE					
25°C RESISTANCE	CERDIP 28-PIN	LCC 28-CONTACT	PLASTIC 28-PIN	TEMPERATURE RANGE			
290Ω	MUX16AT*	-	- "	MIL			
290Ω	MUX16ET	-	_	IND			
400Ω	MUX16BT*	MUX16BTC/883	-	MIL			
400Ω	MUX16FT	_	MUX16FP	XIND			
400Ω	_		MUX16FPC	XIND			
290Ω	MUX28AT*	_	_	MIL			
290Ω	MUX28ET	_	_	IND			
400Ω	MUX28BT*	MUX28BTC/883	_	MIL			
400Ω	MUX28FT	_	MUX28FP	XIND			
400Ω	_		MUX28FPC	XIND			

- For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
- † Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

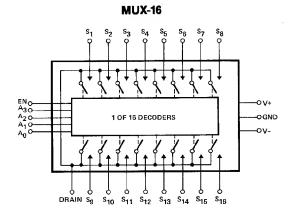
# **GENERAL DESCRIPTION**

The MUX-16 is a monolithic 16-channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package selection function.

The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. A 3-bit binary input address connects a pair of independent analog inputs from each 8-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select function.

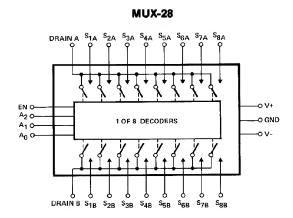
Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static discharge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors. For single 8-channel and dual 4-channel models, refer to the MUX-08/MUX-24 data sheet.

#### **FUNCTIONAL DIAGRAMS**



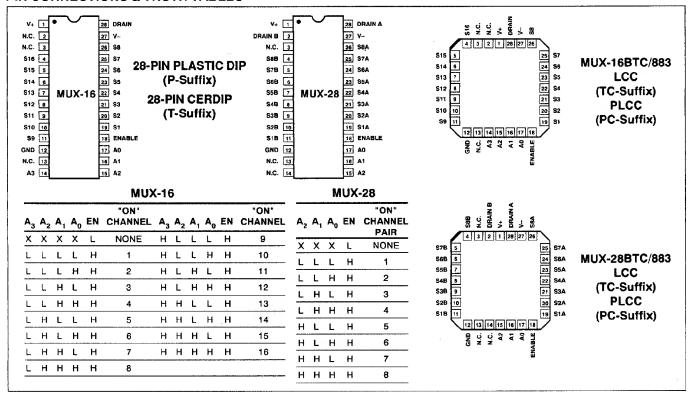
#### REV. A

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# **PIN CONNECTIONS & TRUTH TABLES**



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range

Operating reinperature hange,	
MUX-16/28-AT, BT, BTC	55°C to +125°C
MUX-16/28-ET	25°C to +85°C
MUX-16/28-FP, FPC, FT	40°C to +85°C
Junction Temperature (T <sub>j</sub> ) Storage Temperature Range	65°C to +150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 60 se	ec) 300°C
Maximum Junction Temperature	150°C
V+ Supply to V- Supply	36V
Logic Input Voltage	. (V- or -4V) to V+ Supply
Analog Input Voltage V- Suppl	

Maximum Current Thro	Maximum Current Through Any Pin2							
PACKAGE TYPE	⊖ <sub>jA</sub> (Note 2)	e <sub>jc</sub>	UNITS					
28-Pin Hermetic DIP (T)	55	15	°C/W					
28-Pin Plastic DIP (P)	56	30	°C/W					
28-Contact LCC (TC)	86	35	°C/W					
28-Contact PLCC (PC)	70	33	°C/W					

# NOTES:

- 1. Ratings apply to both DICE and packaged parts, unless otherwise noted.
- Θ<sub>iA</sub> is specified for worst case mounting conditions, i.e., Θ<sub>iA</sub> is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ<sub>iA</sub> is specified for device soldered to printed circuit board for PLCC package.

# **ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15 V$ and $T_A = 25 ^{\circ} C$ , unless otherwise noted.

PARAMETER	SYMBOL CONDITIONS				JX-16/ JX-28/ TYP		MUX-16B/F MUX-28B/F MIN TYP MAX		-	F	
"ON" Resistance	R <sub>ON</sub>	$V_{S} \le 10V, I_{S} \le 200 \mu A$		_	290	380	_	400	580	Ω	
ΔR <sub>ON</sub> With Applied Voltage	$\Delta R_{ON}$	$-10V \le V_S \le 10V$ , $ _S = 200\mu A$			1.5	5		1.5	5	%	
R <sub>ON</sub> Match Between Switches	R <sub>ON</sub> Match	$V_S = 0V, I_S = 200 \mu A$		_	7	<b>1</b> 5	<del>-</del>	9	20	%	
Analog Voltage Range	V <sub>A</sub>	(Note 6)		+10 -10	+ 11 -15	_	+ 10 -10	+ 11 - 15		V	
Source Current (Switch "OFF")	I <sub>S</sub> (OFF)	$V_S = 10V, V_D = -10V \text{ (Note 1)}$		_	0.01	1	_	0.01	2	nA	
Drain Current (Switch "OFF")	I <sub>D</sub> (OFF)	$V_S = 10V, V_D = 110V \text{ (Note 1)}$	MUX-16 MUX-28	_	0.2 0.1	1	_	0.2 0.1	2 2	nA	
Leakage Current (Switch "ON")	I <sub>D</sub> (ON) +I <sub>S</sub> (ON)	V <sub>D</sub> = 10V (Note 1)	MUX-16 MUX-28		0.2 0.1	1	_	0.2	2 2	nA	
Digital Input Current	I <sub>IN</sub>	V <sub>IN</sub> = 0.4V to 15V	-	_	1	10	_	1	10	μΑ	

# **ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$ and $T_A = +25$ °C, unless otherwise noted. Continued

				MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Digital "0" Enable Current	I <sub>INL</sub> (EN)	V <sub>EN</sub> = 0.4V	•	-	4	10	-	4	10	μΑ
Digital Input Capacitance	C <sub>DIG</sub>			-	3	_	_	3	_	pF
Switching Time (t <sub>TRAN</sub> )	t <sub>PHL</sub> t <sub>PLH</sub>	(Notes 2,5) Figure 1 (Test Circuits)	NAME OF THE OWNER OWNER OF THE OWNER	-	1.4 1.2	2.0 1.8	-	1.8 1.6	2.5 2.2	μs
Output Settling Time	t <sub>s</sub>	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%		- - -	2.6 3.2 4.0	- - -	- - -	2.7 3.4 7.2		μs
Break-Before-Make Delay	t <sub>OPEN</sub>	Figure 3			0.7	_	-	1	_	μs
Enable Delay "ON"	t <sub>on (en)</sub>	(Note 5) Figure 2 (Test Circults)		-	1	2		1.2	2.5	μS
Enable Delay "OFF"	t <sub>OFF (EN)</sub>	(Note 5) Figure 2 (Test Circuits)	MUX-16 MUX-28		0.25 0.25	0.5 0.5	- -	0.25 0.25	0.5 0.6	μS
"OFF" Isolation	ISO <sub>OFF</sub>	(Note 4) Figure 4 (Test Circuits)		_	66	_	_	66	-	dB
Crosstalk	СТ	(Note 3) Figure 5 (Test Circuits)		_	75	_	_	75	_	dB
Source Capacitance	C <sub>S (OFF)</sub>	Switch "OFF," V <sub>S</sub> = 0V, V <sub>D</sub> = 0V		_	2.5	_	_	2.5	_	pF
Drain Capacitance	C <sub>D (OFF)</sub>	Switch "OFF,"  V <sub>S</sub> = 0V, V <sub>D</sub> = 0V	MUX-16 MUX-28		13 8	_	_	13 8		pF
Input to Output Capacitance	C <sub>DS (OFF)</sub>	(Note 4)		_	0.15	_	-	0.15	_	pF
Positive Supply Current (All Digital Inputs	I+	V+ = 15V	MUX-16 MUX-28	<del>-</del>	15 15	19 19		9	19 19	mA
Logic "0" or "1")		V+ = 5V	MUX-16 MUX-28		12 12		_	8 7		
Negative Supply Current (All Digital Inputs	I–	V- = -15V	MUX-16 MUX-28	_ _	5 5	7 7	-	3.5 3	7	mA
Logic "0" or "1")	ı–	V-=-5V	MUX-16 MUX-28	<u>-</u>	4 4	_	-	3 2.5	-	ША

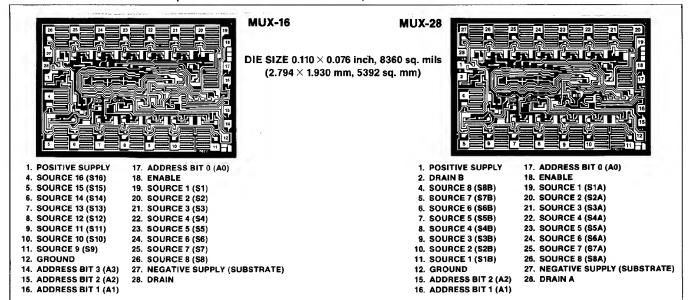
#### NOTES:

- 1. Conditions applied to leakage tests insure worst case leakages.
- 2.  $R_L = 10M\Omega$ ,  $C_L = 10pF$ .
- 3. Crosstalk is measured by driving channel 8 (8B\*) with channel 7 (7B\*) ON.  $R_L=1M\Omega$ ,  $C_L=10pF$ ,  $V_S=5V$  RMS, f=500kHz.
- 4. "OFF" isolation is measured by driving channel 8 (8B) with ALL channels OFF.  $R_L = 1k\Omega$ ,  $C_L = 10pF$ ,  $V_S = 5V$  RMS, f = 500kHz.  $C_{DS}$  is computed from the OFF isolation measurement.
- 5. Sample tested.
- 6. Guaranteed by leakage current and R<sub>ON</sub> tests.

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15 \text{V}$ ,  $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  for MUX-16AT/BT/BTC and MUX-28AT/BT/BTC;  $-25^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  for MUX-16ET and MUX-28ET;  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  for MUX-16 FT/FP/FPC and MUX-28FT/FP/FPC, unless otherwise noted.

			MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
"ON" Resistance	R <sub>ON</sub>	V <sub>S</sub> ≤ 10, I <sub>S</sub> ≤ 200μA	-	-	500	-	-	800	Ω
ΔR <sub>ON</sub> With Applied Voltage	ARON	-10V ≤ V <sub>S</sub> ≤ 10V, I <sub>S</sub> = 200μA	_	2	- *	_	5.5		%
R <sub>ON</sub> Match Between Switches	R <sub>ON</sub> Match	V <sub>S</sub> = 0V, I <sub>S</sub> = 200μA	-	10	_	_	15	-	%
Analog Voltage Range	V <sub>A</sub> .	(Note 6)	+10 -10	+11 -15	_	+10 -10	+11 -15	<u>-</u>	V
Source Current (Switch*OFF*)	I <sub>S (OFF)</sub>	$V_{S} = 10V, V_{D} = -10V \text{ (Note 1)}$	-	-	25	_	_	50	nA
Drain Current (Switch "OFF")	I <sub>D</sub> (OFF)	V <sub>S</sub> = 10V, V <sub>D</sub> = -10V (Note 1)		_	75	_	_	250	пА
Leakage Current (Switch "ON")	I <sub>D</sub> (ON) +I <sub>S</sub> (ON)	V <sub>D</sub> = 10V (Note 1)	***	-	75	_	_	250	nA
Digital "1" Input Voltage	V <sub>INH</sub>	(Note 6)	2	-	-	2	_	_	٧
Digital "0" Input Voltage	V <sub>INL</sub>	(Note 6)	-	_	0.7	_	-	0.7	V
Digital Input Current	I <sub>IN</sub>	V <sub>IN</sub> = 0.4V to 15V	_	_	20	_	_	20	μА
Digital "0" Enable Current	I <sub>INL</sub> (EN)	V <sub>EN</sub> = 0.4V	_	_	20			20	μΑ
Positive Supply Current	l+	All Digital Inputs Logic "0" or "1"		_	24	_	_	24	mA
Negative Supply Current	1-	All Digital Inputs Logic "0" or "1"	_	_	8.2	_	-	8.2	mA

# DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



**WAFER TEST LIMITS** at V + = 15V, V - = -15V,  $T_A = 25^{\circ}$  C for MUX-16/28 N and G,  $T_A = 125^{\circ}$  C for MUX-16/28 NT and GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT LIMIT	MUX-16/ MUX-28N LIMIT	MUX-16/ MUX-28GT LIMIT	MUX-16/ MUX-28G LIMIT	UNITS
"ON" Resistance	R <sub>ON</sub>	$V_S = 0V,$ $I_S = 200 \mu A$	540	380	800	580	Ω ΜΑΧ
Digital "1" Input Voltage	V <sub>INH</sub>		2	2	2	2	V MIN
Digital "0" Input Voltage	V <sub>INL</sub>	The second of th	0.8	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I <sub>INL</sub>	V <sub>IN</sub> = 0.4V	20	10	20	10	μΑ ΜΑΧ
Digital "0" Enable Current	INL(EN)	V <sub>EN</sub> = 0.4V	20	10	20	10	μΑ ΜΑΧ
Positive Supply Current (All Digital Inputs Logic "0")	I+		24	19	24	19	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I-		8.2	7	8.2	7	mA MAX
Analog Input Range	V <sub>A</sub>	(Note 2)	±10	±10	±10	±10	V MIN

#### NOTE

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at V+=15V, V-=-15V and  $T_A=25^{\circ}$  C for MUX-16/28 N and G,  $T_A=125^{\circ}$  C for MUX-16/28 NT and GT, unless otherwise noted.

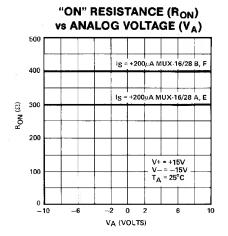
PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT TYPICAL	MUX-16/ MUX-28N TYPICAL	MUX-16/ MUX-28GT TYPICAL	MUX-16/ MUX-28G TYPICAL	UNITS
Switching Time (t <sub>TRAN</sub> )	t <sub>PHL</sub>	(Note 1) Figure 1	2 1.8	<b>1</b> 0.9	2.6 2.4	1.5 1.4	μ
Output Settling Time	t <sub>S</sub>	10V Step to 0.1% (Note 1)	2.5	1.5	2.9	1.9	μs
Break-Before-Make Delay	t <sub>OPEN</sub>	(Note 1) Figure 3 (Test Circuits)	0.8	0.8	1	1	μs
Crosstalk	СТ	(Note 1) Figure 5 (Test Circuits)	70	70	70	70	dB
ΔR <sub>ON</sub> With Applied Voltage	$\Delta R_{ON}$	$-10V \le V_S \le 10V$ , $ _S = 200 \mu A$	1.5	1.5	1.5	1.5	%
Leakage Current (Switch "ON")	I <sub>D (QN)</sub>	V <sub>D</sub> = 10V (Note 1)	20	0.2	20	0.2	nA
Analog Input Range	V <sub>A</sub>	(Note 2)	+ <b>1</b> 1 - <b>1</b> 5	+11 -15	+11 -15	+11 -15	V

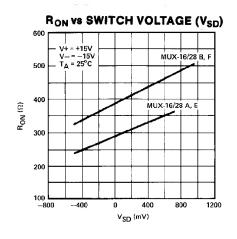
#### NOTES:

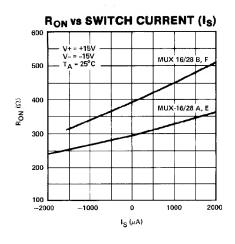
The data shown is extrapolated from measurements made on the packaged devices.

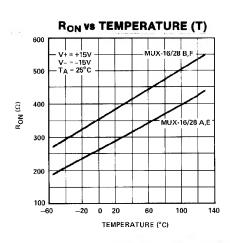
<sup>2.</sup> Guaranteed by R<sub>ON</sub> and leakage current tests.

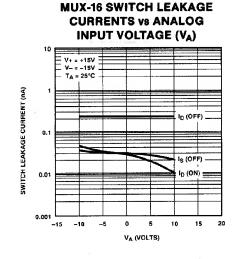
# TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

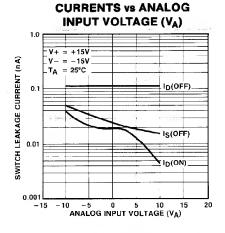




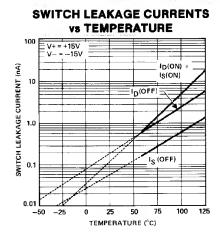


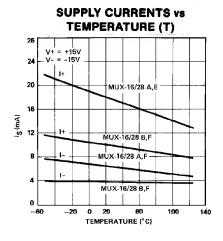


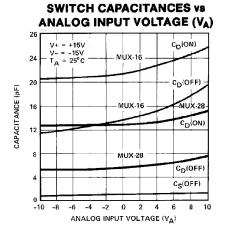




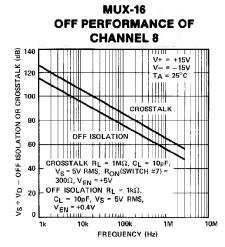
**MUX-28 SWITCH LEAKAGE** 

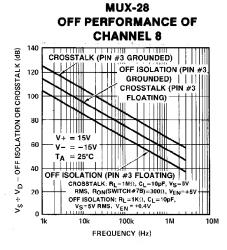


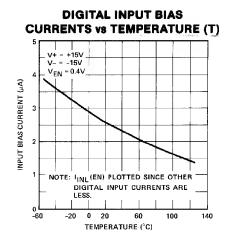




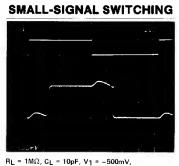
# TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)





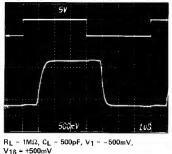


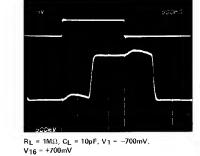
#### **MUX-16 DYNAMIC CHARACTERISTIC CURVES**





# **SMALL-SIGNAL SWITCHING** WITH FILTERING 5V

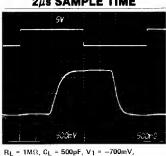




**SMALL-SIGNAL SWITCHING** 

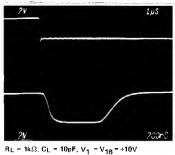
WITH 2µ\$ SAMPLE TIME

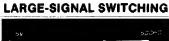


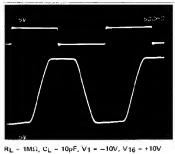


 $R_L = 1M\Omega$ ,  $C_L = 500pF$ ,  $V_1 = -700mV$ ,  $V_{16} = +700mV$ 

# **BREAK-BEFORE-MAKE SWITCHING**







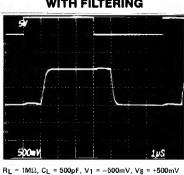
# NOTE:

Top Waveforms: Digital Input 5V/Div Bottom Waveforms: Multiplexer Output (VD)

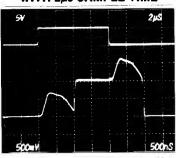
# **MUX-28 DYNAMIC CHARACTERISTIC CURVES**

# **SMALL-SIGNAL SWITCHING** $R_L$ = 1M $\Omega$ , $C_L$ = 10pF, $V_1$ = -500mV, $V_8$ = +500mV

# **SMALL-SIGNAL SWITCHING** WITH FILTERING

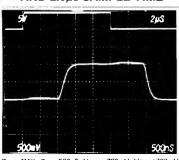


**SMALL-SIGNAL SWITCHING** WITH 2µ8 SAMPLE TIME

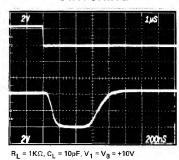


 $R_L = 1M\Omega$ ,  $C_L = 10pF$ ,  $V_1 = -700mV$ ,  $V_8 = +700mV$ 

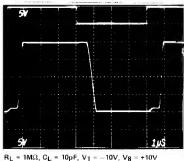




**BREAK-BEFORE-MAKE SWITCHING** 



**LARGE-SIGNAL SWITCHING** 

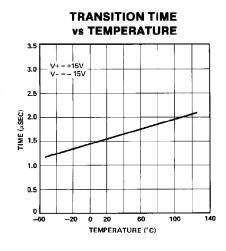


 $R_L = 1M\Omega$ ,  $C_L = 500pF$ ,  $V_1 = -700mV$ ,  $V_8 = +700mV$ 

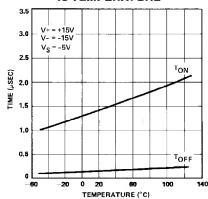
# NOTE:

Top Waveforms: Digital Input 5V/Div Bottom Waveforms: Multiplexer Output (VD)

# TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

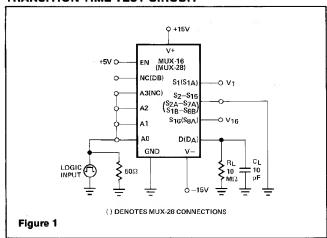




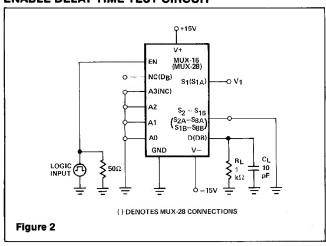


# A.C. TEST CIRCUITS

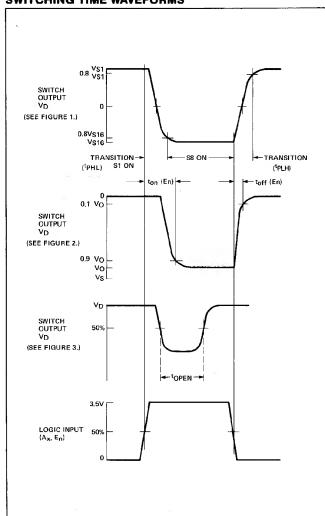
# TRANSITION TIME TEST CIRCUIT



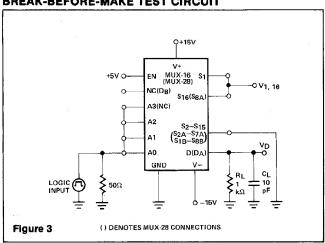
# **ENABLE DELAY TIME TEST CIRCUIT**



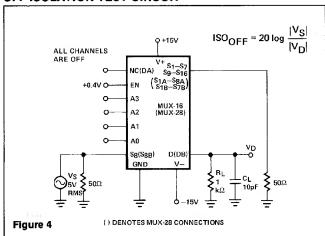
# **SWITCHING TIME WAVEFORMS**



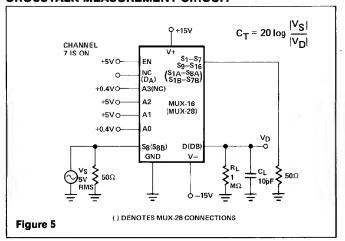
# **BREAK-BEFORE-MAKE TEST CIRCUIT**



# **OFF ISOLATION TEST CIRCUIT**



#### **CROSSTALK MEASUREMENT CIRCUIT**



# V<sub>EN</sub> O E<sub>N</sub> V+ S16(S8A) NC(DB) S1-S15 (S1A-S7A) A3(NC) (S1B-S8B) A2 A1 D(DA) A0 GND V 1MΩ E VA (1) DENOTES MUX-28 CONNECTIONS

**OVERVOLTAGE MEASUREMENT TEST CIRCUIT** 

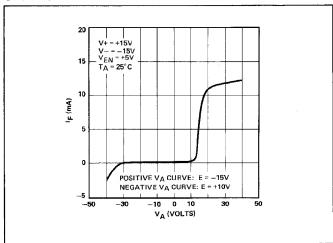
## **APPLICATIONS INFORMATION**

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make (B.B.M.) action. The turn-off time is much faster than the turn-on time to guarantee B.B.M. over the full operating temperature and input voltage range. Fabricated with JFET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above ≈ 1.4V.

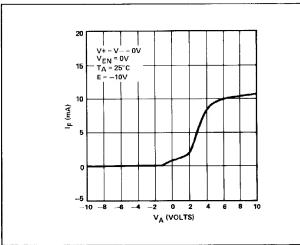
The "ON" resistance,  $R_{ON}$  of the analog switches is constant over the wide input voltage range of -15V to +11V with  $V_{SUPPLY}=\pm15V$ . The overvoltage and supply-loss V-I characteristics shown indicate typical performance when the multiplexer is subjected to abnormal signals. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the  $V_{GS}$  of an OFF FET switch remains greater than its  $V_P$ , preventing that channel from being falsely turned ON.

When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds –0.6V. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a  $0.01\mu F$  capacitor in the circuit of Figure 1. With  $V_1=-10V$  and  $V_{16}=+10V$ , the logic input was driven at a 1kHz rate. The positive-going slew rate was  $0.3V/\mu Sec$  which is equivalent to a normal  $I_{DSS}$  of 3mA. The negative-going slew rate was  $0.7V/\mu sec$  which is equivalent to a "reverse"  $I_{DSS}$  of 7mA. Note that when switch one (1) is first turned ON it has a drop of –20V across its terminals. In spite of that fact, the current is limited to approximately twice its normal  $I_{DSS}$ .

# **OVERVOLTAGE V-I CHARACTERISTIC**



# SUPPLY-LOSS V-I CHARACTERISTIC



# **SIMPLIFIED SCHEMATIC (MUX-16)**

